the P type RESURF layer **315**, the equipotential lines are restricted from entering the P type base region **303** more effectively than a portion between the stripe portions of the P type deep layer **310**.

[0240] Thus, the equipotential lines are substantially horizontal to the planer direction of the N+ type substrate **301** at the portion between the P type deep layer **310** and the P type RESURF layer **315**, and the electric field applies in the vertical direction of the planer direction of the N+ type substrate **301**, that is, in the direction of the (0001)-face. Therefore, the SiC semiconductor device according to the present embodiment can have effects similar to the effects of the SiC semiconductor device according to the sixth embodiment.

[0241] In addition, in the SiC semiconductor device according to the present embodiment, a clearance is provided between the P type deep layer **310** and the P type RESURF layer **315**. Because the P type deep layer **310** and the P type RESURF layer **315** are formed at different processes, the P type deep layer **310** may overlap the P type RESURF layer **315** due to misalignment of masks. However, by providing the clearance between the P type deep layer **310** and the P type RESURF layer **315**, the overlap of the P type deep layer **310** and the P type RESURF layer **315** due to the misalignment of the masks can be restricted. If the P type deep layer **310** overlaps the P type RESURF layer **315** and the impurity concentration increases, the equipotential lines may be distorted and the electric field concentration may occur. However, by providing the clearance between the P type deep layer **310** and the P type RESURF layer **315**, the electric filed concentration can be restricted.

Eighth Embodiment

[0242] An SiC semiconductor device according to an eighth embodiment of the present invention will be described with reference to FIG. **36**, FIG. **37**A, and FIG. **37**B.

[0243] In the SiC semiconductor device according to the present embodiment, the outer edge portion of the P type deep layer **310** reaches the P type RESURF layer **315**. However, a plurality of openings **310***a* in which the P type deep layer **310** is not formed is provided at the outer edge portion of the P type deep layer **310**. A dimension of each of the openings **310***a* is less than the intervals of stripe portions of the P type deep layer **310**. For example, each of the openings **310***a* has an approximately square shape and each side of the approximately square shape is less than the intervals of the stripe portions of the P type deep layer **310**. Each of the openings **310***a* may have another shape. In a case where each of the openings **310***a* has an approximately circular shape, a diameter of the approximately circular shape is less than the intervals of the stripe portions of the P type deep layer **310**.

[0244] Although the openings **310***a* are provided in the outer edge portion of the P type deep layer **310**, the dimension of each of the openings **310***a* is set to be less than the intervals of the stripe portions of the deep layer **310**. Thus, the depletion layer expanding from the outer edge portion of the P type deep layer **310** fills the openings **310***a* when the voltage is not applied to the gate electrode. Therefore, the SiC semiconductor device according to the present embodiment can have effects similar to the effects of the SiC semiconductor device according to the sixth embodiment.

Ninth Embodiment

[0245] An SiC semiconductor device according to a ninth embodiment of the present invention will be described with reference to FIG. **38**A and FIG. **38**B.

[0246] In the SiC semiconductor device according to the present embodiment, the P type deep layer **310** is connected with the P type RESURF layer **315**. The P type deep layer **310** and the P type RESURF layer **315** has the same depth and the same impurity concentration. The P type RESURF layer **315** is not formed at the sidewall of the stepped part of the mesa structure portion **314**. The P type base region **303** is formed to the boundary portion between the cell section Sa and the peripheral section Sb.

[0247] An exemplary method of manufacturing the SiC semiconductor device according to the present embodiment will be described with reference to FIG. **39**A to FIG. **39**B. A process illustrated in FIG. **39**A is performed in a manner similar to the process illustrated in FIG. **33**A. A process illustrated in FIG. **39**B is performed in a manner similar to the process illustrated in FIG. **33**B. However, during the process illustrated in FIG. **39**B, the P type RESURF layer **315** is formed at the surface portion of the N− type drift layer **302** in addition to the P type deep layer **310** and the P type guard ring layers **316**. The P type RESURF layer **315** is formed so as to be connected with the P type deep layer **310**. A process illustrated in FIG. **39**C is performed in a manner similar to the process illustrated in FIG. **33**C. During a process illustrated in FIG. **39**D, the mesa structure portion **314** is formed in a manner similar to the process illustrated in FIG. **33**D. A process illustrated in FIG. **39**E is performed in a manner similar to the process illustrated in FIG. **33**E. Thereby, the SiC semiconductor device according to the present embodiment is formed.

[0248] As described above, the P type RESURF layer **315** can be formed at the same time with the P type deep layer **310**. The SiC semiconductor device according to the present embodiment can have effects similar to the effects of the SiC semiconductor device according to the sixth embodiment. In addition, the process for forming the P type RESURF layer **315** and the P type deep layer **310** can be simplified. Furthermore, an overlap of the P type RESURF layer **315** and the P type deep layer **310** can be prevented, and thereby the electric field concentration due to a distortion of the equipotential lines can be restricted. Therefore, the SiC semiconductor device according to the present embodiment can have effects similar to the effects of the SiC semiconductor device according to the seventh embodiment.

[0249] Each of the SiC semiconductor devices according to the sixth to ninth embodiments includes the N-channel type MOSFET, as an example. Alternatively, the SiC semiconductor devices may include a P-channel type MOSFET in which conductivity types of the components are reversed. Alternatively, the SiC semiconductor devices may include insulated gate bipolar transistors (IGBTs) each having a trench gate structure. In a case where the SiC semiconductor devices include the IGBTs, the conductivity type of the N+ type substrate **301** is changed from the N conductivity type to the P conductivity type. Other structure and a manufacturing method are similar to the method described in the sixth embodiment.

[0250] In each of the SiC semiconductor devices according to the sixth to ninth embodiments, the gate oxide layer **308** formed by the thermal oxidation is provided as an example of a gate insulating layer. Alternatively, the gate insulating layer may be an oxide layer formed by another method or a nitride layer, for example. The drain electrode **313** may be formed after forming the source electrode **311**.